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EXAMINER	
SHEW, JOHN	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,900	GRIVNA, EDWARD L.	
	Examiner	Art Unit	
	John L Shew	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4-6,11-17,20 and 21* is/are rejected.

7)☒ Claim(s) *7-10 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 3 and 18 are withdrawn in view of the newly discovered reference(s) to Le et al. Rejections based on the newly cited reference(s) follow.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore regarding FIG. 3, the claim 12 limitation of "SRAM" must be shown or the feature(s) canceled from the claim(s), and
the claim 13 limitation of "two banks of standard RAM" must be shown or the feature(s) canceled from the claim(s).
No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 15, 20 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the criteria on amount of bit errors allowed while method is in framing status before framing is lost.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See

MPEP § 2172.01. The omitted steps are: wherein the method allows a reframe there is no relationship to the prior method limitations and no steps on the formulation of the reframing method.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 6, 11-13, 14, 15-17, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pawlowski (Patent 5854794), in view of Le et al. (Patent 6079001).

Claim 1, Pawlowski teaches an apparatus (FIG. 1) referenced by Data Transmission Framing System, comprising a memory (FIG. 1) referenced by RAM 15, configured to (i) read and/or write (FIG. 1) referenced by EN_RAM signal 20 and RAM_WR signal 21, a plurality of state vectors (FIG. 1) referenced by MUX 11 of vectors from INCR LOGIC 7 and XLATE LOGIC 9, and (ii) read and/or write data (FIG. 1) referenced by DATA SHIFT 4, an encoder configured to present state vectors (FIG. 1) referenced by MUX 11 to encode the selection of RAM data, to be written in response to (i) data read from said memory (FIG. 1) referenced by Latch 6 of data read from RAM 15 into INCR LOGIC 7

XLATE LOGIC 9 and DATA SHIFT 4, (ii) a first address (FIG. 1) referenced by PCM Counter 23 for address of RAM 15, and (iii) a serial data stream (FIG. 1) referenced by serial data SP_DAT 2, one or more registers configured to present said first address in response to an input address (FIG. 1) referenced by Frame Counter 25 as a register to count input address of PCM Counter 23 for 4 cycles. Pawlowski does not teach an address register to store a first address and present a second address.
Le teaches an address register configured to store said first address and present a second address (FIG. 7, FIG. 10) referenced by Address Enable Latch 171 to store a first address and Address Enable Latch 181 to present a second address.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory access method of Le to the digital framing system of Pawlowski for the purpose of accessing slow memory cores sequentially and more efficiently.

Claim 2, Pawlowski teaches a counter circuit configures to generate said input address (FIG. 1) referenced by PCM Counter 23 as circuit to provide said input address.

Claim 4, Pawlowski teaches said encoder further comprises a state machine (FIG. 1) referenced by RD/WR State Machine 18, configured to (i) a monitor for one or more pattern match conditions (column 5 lines 59-65) referenced by monitor of ESF transmission for assertion of Frame Alignment Enable on frame out of alignment to trigger pattern match of ESF Pattern Register 32, (ii) continue to monitor said serial

stream for both valid and invalid pattern match conditions (column 5 line 66-67, column 6 lines 1-4, column 7 lines 20-32) referenced by monitor of serial data stream for ESF framing pattern followed by storage of reference pointer in RAM else a dummy value of 7 is stored, and (iii) continue to monitor for said pattern match conditions and implement a count bit field to track said pattern match conditions and one or more non-match conditions (TABLE 4) referenced by Translation Logic to translate the pattern detection to a reference pointer corresponding to the position of the alignment pattern detected so far else the contents reflect "111" as no frame bits detected, a compare circuit configured to (i) control said state machine (FIG. 1) referenced by XOR gate 36 to compare the SP_DATA 2 with the ESF Pattern Register 32, and (ii) compare said register address and said second address (FIG. 1) referenced by address from PCM Counter 23 and subsequent address from Frame Counter 25 to decode for MUX selection, a gate configured to control said state machine in response to a bit of said data read and said serial data stream (FIG. 1) referenced by Flip Flop 1 latching serial data SP_DAT 2 to control MUX 30 as part of state machine along with Latch 6 of prior data from RAM 15 as part of state machine .

Claim 5, Pawlowski teaches said state machine comprises a first logic section configured to increase a value representing the number of sequential bits found that match a framing pattern (FIG. 1, column 7 lines 63-67, column 8 lines 1-12, TABLE 5) referenced by INCR LOGIC 7 pointer increment as framing pattern is matched, and a second logic section configured to determine if an incrementer is tracking one or more

framing sequence matches or mismatches (FIG. 1) referenced by XOR gate 36 to determine a match or mismatch to ESF Pattern Register 32 with ESF_MTCH signal to INCR LOGIC 7, and if framing has been validated (FIG. 1) referenced by Validation Counter 39 for resulting ESF_VLD signal.

Claim 6, Pawlowski teaches said state machine is configured to simultaneously validate framing at all possible location in a serial stream (FIG. 1, column 2 lines 40-47, column 5 lines 6-12) referenced by a vector for each address entry all 193 possible bit stream positions.

Claims 11-13, Pawlowski teaches said memory comprises a synchronous RAM (FIG. 1) referenced by RAM 15, said memory comprises a RAM with read-modify-write access (FIG. 1) referenced by read data 17 modify input data 16 and write signal RAM_WR 21 wherein such functionality performs as a DPRAM. The functionality of DPRAM can obviously be implemented equivalently as SRAM or standard RAM with associated circuitry for simultaneous reading and/or writing. Pawlowski teaches said memory comprises two banks of standard RAM (FIG. 1) referenced by RAM 15 partitioned as 4 sections which is representative of two banks of two sections each, wherein the first bank is accessed for sequential read operational and a second bank is accessed for sequential write operations (FIG. 1) referenced by signal EN_RAM 20 for read capability and signal RAM_WR 21 for write capability.

Claim 14, Pawlowski teaches said memory comprises a FIFO (FIG. 1) referenced by memory RAM 15 addressed by a PCM Counter 23 in sequential count, having a character depth of at least that of an interleave depth (FIG. 1) referenced by RAM 15 having 193 addressable locations in 4 partitions to correspond to 193x4 bits of interleave depth of extended superframe, and a character width of at least that of a normal state vector (FIG. 1) referenced by width of each addressable location to 3 bits to point to pattern match location, plus one more bit serving as an interleave boundary marker (FIG. 1) referenced by bit ESF_FRM0 40 representing a frame match to identify the interleave boundary marker.

Claims 15-17, Pawlowski teaches a method for detection of framing (column 2 lines 17-21) referenced by framing system using memory pointers to match a framing pattern reference, in a bit interleaved data stream (column 3 lines 23-27) referenced by Extended Super Frame format of bit interleaved data stream, comprising the steps of (A) reading and/or writing (FIG. 1) referenced by EN_RAM signal 20 and RAM_WR signal 21, a plurality of state vectors (FIG. 1) referenced by MUX 11 of vectors from INCR LOGIC 7 and XLATE LOGIC 9, (B) presenting data to be written (FIG. 1) referenced by MUX 11 to encode the selection of RAM data, in response to (i) data read (FIG. 1) referenced by Latch 6 of data read from RAM 15 into INCR LOGIC 7 XLATE LOGIC 9 and DATA SHIFT 4, (ii) a first address (FIG. 1) referenced by PCM Counter 23 for address of RAM 15, and (iii) a serial data stream (FIG. 1) referenced by serial data SP_DAT 2, and (C) presenting said first address in response to an input address (FIG.

1) referenced by PCM Counter 23 presentation of address in response to an address clock SP_CLK, wherein said method retains framing in the presence of bit errors (column 1 lines 62-67, column 2 lines 1-5) referenced by a comparison of only a portion of the transmission frame pattern which allows errors and false framing.
Pawlowski teaches said method simultaneously validates framing at all possible location in a serial data stream (FIG. 1, column 2 lines 40-47, column 5 lines 6-12) referenced by a vector for each address entry all 193 possible bit stream positions.
Pawlowski teaches said method postpones indication of valid framing until a single framing match is present (FIG. 1) referenced by indication signal ESF_VLD when a single framing match is present.

Claim 20, Pawlowski teaches an apparatus (FIG. 1) referenced by Data Transmission Framing System, comprising means for storing a plurality of state vectors (FIG. 1) referenced by memory RAM 15 to store state vectors, means for presenting state vectors to be written (FIG. 1) referenced by MUX 11 presenting state vectors for writing into RAM, in response to (i) data read (FIG. 1) referenced by data read from Latch 6, (ii) a first address (FIG. 1) referenced by PCM Counter 23 for address of RAM 15, and (iii) a serial data stream (FIG. 1) referenced by serial data SP_DAT 2, and means for presenting said first address in response to an input address (FIG. 1) referenced by PCM Counter 23 presentation of address in response to an address clock SP_CLK, wherein said method retains framing in the presence of bit errors (column 1 lines 62-67,

column 2 lines 1-5) referenced by a comparison of only a portion of the transmission frame pattern which allows errors and false framing.

Allowable Subject Matter

4. Claims 7-10, 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Citation of Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patent 6654368, Smith discloses an apparatus for processing frame structured data signals.

Response to Arguments

5. Applicant's arguments filed 09/22/2004 regarding drawing objections have been fully considered but they are not persuasive. Drawing objections are maintained. The embodiment of the invention as presented in FIG. 3 clearly identifies the memory component 104 as a DPRAM. Claim 12 carry a limitation of said memory comprises a SRAM, while claim 13 carry a limitation of said memory comprises two banks of RAM. This presents a conflict of the embodiment as presented with the claims. It is suggested to modify FIG. 3 to use a generic memory element instead of the DPRAM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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